Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (Chairperson)

Session Chair	Dr. GOH Szu Huat
Company	GLOBALFOUNDRIES Singapore Pte Ltd, Singapore
Designation	Senior Manager, Product Diagnostics Engineering
Biography 	Szu Huat received his BEng and PhD in electrical and computer engineering from the National University of Singapore. His doctorate research on simulation and implementation of aplanatic refractive solid immersion lens was awarded a conference best paper and part of a team project that received the 2009 Singapore President's Technology award. He co-worked with the team members from an SME to commercialize the lens in 2009. Dr Goh is currently with GLOBALFOUNDRIES, Product, Test and Failure Analysis division, Singapore, where he leads a team responsible for product failure diagnostics and advanced methodologies to accelerate yield ramp. His main focus is on the development of dynamic fault isolation techniques, wafer level fault isolation methods and leveraging cross-functional domain knowledge of design, test and failure analysis to enhance yield learning. His works have been published in conferences and journals. Together with his team, he invented a new technique called Electrically-enhanced LADA which was accorded a conference best paper in 2015. Szu Huat has been a tutorial speaker for the past 3 years for the International Symposium for Testing and Failure Analysis (ISTFA) US conference. He is also the technical program chair for the International Physical and Failure Analysis (IPFA) in 2016.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (10:00-10:25hrs)

Speaker	Dr. HUA Younan
Company	WinTech Nano-Technology Services Pte Ltd, Singapore
Designation	Vice President & Chief Operation Officer
Title of Presentation	**Studies and Application of New FA Technique for Gate Oxide Integrity (GOI) Failure in Semiconductor Manufacturing and Wafer Fabrication**
Abstract	As device feature sizes continue to shrink, the reducing gate oxide thicknesses put more stringent requirements on gate dielectric quality in terms of defect density and contamination concentration. As a result, analyzing gate oxide integrity and dielectric breakdown failures during wafer fabrication becomes more difficult. Traditional FA flow is able to locate the defects using electrical fault isolation methods such as OBIRCH, TIVA and EMMI, whereas the root cause of failure can hardly be uncovered. This course will introduce the latest techniques for GOI failures analysis with high success rate, in which the EFA techniques (OBIRCH, TIVA and EMMI), chemical Wright Etch, TOF-SIMS, VPD ICP-MS and D-SIMS are combined to use for the root cause identification. EFA technique is used for fault isolation to locate the defects, while chemical Wright Etch is used for failure mode identification in general. The shape of Si crystalline defect delineated by Wright Etch can help identify whether the GOI failure is related to PID (Plasma-Induced Damage) or contamination. In the event of contamination induced failure, TOF-SIMS or VPD ICP-MS are used for contamination survey. Finally D-SIMS is used to further determine the contamination source and concentration level (ppm-ppt). In this course, some GOI FA case-studies will be presented. Moreover, in order to prevent or reduce GOI failure in semiconductor manufacturing, wafer fab in-line process quality control, baseline measurement, establishment of Control/Spec Limit and monitoring procedure will also be discussed.
Biography 	Dr. Hua Younan received his Ph. D degree in Physics from National University of Singapore in 1994. He currently serves as a Vice-President/Chief Operation Officer in WinTech Nano-Technology Service Pte Ltd (Singapore), which is a worldwide leading analytical services company. Dr Hua's professional background includes services in both technical and management positions. From 1995 to 2013, he served at GLOBALFOUNDRIES Singapore (formerly Chartered Semiconductor) as a Quality Director with experience in quality assurance and failure analysis (including SEM/EDX, FIB, TEM, D-SIMS, TOF-SIMS, Auger, XPS, FTIR, AFM, XRD, VPD/ICP-MS, GC-MS, IC, etc.). Before joining Chartered Semiconductor/GLOBALFOUNDRIES, Dr Hua served at the National University of Singapore and Nanjing Institute for 13 years. In total, he has more than 35 years of working experience in material science, engineering research, failure analysis for semiconductor and wafer fab. He has published more than 300 technical papers and filed 5 patents.

	Dr Hua has conducted deep theoretical studies in FA techniques in semiconductor and wafer fab, microchip Al bondpad corrosion and eliminating solutions, chemical deprocessing techniques and elimination of Si crystalline defects, energy-dispersive X-ray microanalysis, X-ray fluorescence analysis and surface analysis (Auger, XPS and SIMS etc.). He has developed the latest new FA flow of GOI failure, in which several FA techniques (including EFA, chemical FA and surface FA) are combined to use for root cause identification of GOI failure and greatly improve FA success rate and reduce overall FA turnaround time and cost. Dr Hua is a member of National University of Singapore Consultative Committee (MSE, 2017-2108); Co-supervisor of Ph.D students with Singapore EDB-WinTech-NUS/NTU/SUTD IPP Platform and IEEE IPFA International Conference Organizing Committee Member/Co-Chair (2012, 2014 and 2016). He is Vice-president of Jiangsu Association (Singapore) and is enthusiastic about social welfare and charitable activities in Singapore.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (10:25-10:50hrs)

Speaker	Dr. Andrew Jonathan SMITH
Company	Kleindiek Nanotechnik, Germany
Designation	Sales and Application Specialist
Title of Presentation	**Electronic Fault Isolation on Cutting-Edge Technology Nodes - NanoProbing in Failure Analysis**
Abstract	Addressing the challenges in locating and characterizing faults and failures at contact level in current node technology requires a powerful SEM capable of imaging nanostructures at low beam energies AND an extremely precise and stable set of nanomanipulators equipped with sharp probe tips in order to contact the sample. Once contact has been achieved, a number of analysis techniques and tools can be employed to narrow-in on the problem and/or further characterize the issue at hand. A number of these techniques will be introduced in this work.
Biography 	Andrew studied chemistry at the Heinrich-Heine University Düsseldorf after which he prepared his doctoral thesis on single crystalline tungsten nanowires at the Max-Planck-Institut für Eisenforschung. After receiving his PhD, he joined Kleindiek Nanotechnik as a sales and application specialist.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (11:15-11:40hrs)

Speaker	Mr. Larry DWORKIN
Company	Thermo Fisher Scientific, USA
Designation	Director, Business Development
Title of Presentation	**Improving Time to Data for TEM Sample Preparation and Analysis**
Abstract	In the Age of IoT it is critical that device manufacturers be able to improve the yield ramp and minimize time to market for their products. The path to improving yield relies on being able to determine root cause analysis for critical defects as quickly as possible. As devices become smaller and more complex determining root causation relies increasingly on TEM data. The need to improve time to data as well as the increasing volume demands has driven requirements for automation of TEM sample preparation and analysis. In this presentation we will discuss the methods for improving time to data for TEM including bring DualBeams and TEMs into the fab, ways of reducing the complexity of tasks an operator must perform to prepare and analyze a TEM sample, and how to lower operating costs by enabling a single operator to utilize multiple systems simultaneously.
Biography 	Larry Dworkin is the Director of Business Development and Field Applications in the semiconductor business unit at Thermo Fisher Scientifc. He has worked at Thermo Fisher Scientific for over 15 years in several sales and marketing roles. As a Product Marketing Manager he launched both the Helios Nanolab 1200 wafer DualBeam and the Metrios TEM. His current focus is on developing high value analytical solutions for electrical and physical failure analysis. Prior to joining Thermo Fisher Scientific he worked at Applied Materials on defect reduction of BEOL module development. Dworkin received a MS degree in Physics from University of California, Los Angeles.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (11:40-12:05hrs)

Speaker	Ir. Dr. Norhayati SOIN
Company	University of Malaya, Malaysia
Designation	Associate Professor
Title of Presentation	**Physical Unclonable Function (PUF)-Security Enabled FPGA for Medical Solutions in IoT**
Abstract	The development of technology, coupled with medical advances, have enabled the realization of digital healthcare to reduce inefficiencies in health care delivery and improve patient access, which in turn suppress the pressure of healthcare system at a world-wide scale. Wireless communication is widely used to facilitate real time monitoring. However, these wireless devices are easy targets for malicious hacks and hence impose a danger to the life of a patient. Our research aims to develop a novel security function embedded in digital electronics technology, and further integrated into existing wireless medical instruments. Ultimately, this can provide practical and costless solution in the digital healthcare sector. The ultimate goal of this research is to provide a secure solution in the growing innovation of Internet-of-things (IoT), specifically the healthcare sector. Wireless technology has made communication with medical instruments easier and safer for medical practitioners, though security risks have also emerged. A majority of medical devices implement little to no command authorization and encryption schemes thus exposing the devices to malicious attackers that can remotely extract sensitive information from these devices or even be able to take control of the devices and issues threatening commands. Hence it is critical to enforce security of medical device wireless communication such as that of the shared key derivation encryption by employing PUFs. The aim of the proposed research is to design a security key in the form of a Physical Unclonable Function (PUF) and integrate this physical entity into a commercial-on-the-shelf (COTS) field programmable gate array (FPGA) chip. The PUF-based COTS FPGA chip is further integrated into existing wireless medical equipment used in hospitals and healthcare centers. The **ambition** is to, for the first time, provide a feasible, practical and costless solution for digital healthcare industry.

Biography	Ir. Dr. Norhayati Soin received the B. Eng. (Hons) degree in electrical and electronics engineering from the Liverpool Polytechnic, United Kingdom and MSc degree in Microelectronics Engineering from Liverpool John Moores University, United Kingdom. She has then received her PhD degree in Electronics and Systems Engineering from National University of Malaysia. She is currently an Associate Professor with the Department of Electrical Engineering, University of Malaya, Malaysia. Her research interests include semiconductor device and integrated circuits reliability, MEMS design and fabrication. She is a Professional Engineer certified by the Board of Engineer Malaysia (BEM). She now leads the VLSI Reliability Research Group and Center of Printable Electronics in University Malaya. She is a senior member of IEEE and IEEE Electron Devices. She is currently the vice chair of the IEEE Electron Devices Malaysia Chapter. She has published more than 100 International Journal and Conference papers. She is/was a member of the program committee of several international conferences. She is the principal investigator for local and international research projects on lifetime prediction of semiconductor devices and integrated circuits.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (12:05-12:30hrs)

Speaker	Mr. Mike von den HOFF
Company	KLA-Tencor Corporation, Europe
Designation	Senior Yield Consultant
Title of Presentation	**RMA Root Cause Investigation 20nm Technology**
Abstract	This paper describes the methodology, results and improvements for defect reduction in the Front End of Line of a 20nm planar technology. The defect inspection optimization and defect reduction methodology were implemented for the High-k Metal Gate (HKMG) stack module on 300mm wafers on high performance logic devices. Along with new technological advances, reduction of critical defects becomes increasingly important. The introduction of multi-level HKMG stack material is a significant challenge in terms of yield limiting and latent reliability defects. The multiple materials interfaces lead to an increased variety of defect mechanisms in the gate module. As a consequence, defect management in the gate stack has become critical to successful yield ramp and to avoid critical reliability defects. From a defect management perspective, HKMG stack has some unique characteristics. Very small defects in the gate module at earlier steps can lead to larger and more yield relevant defects at later steps as layers are deposited on each other. Similarly, these types of defects may be marginal and not even been detected at final probe – but are a significant risk for latent reliability issues. Fig. 1 shows two critical HKMG defects. Both defect have the same source and similar size – but while one defect is causing a short and get detected at probe, the second defect barriers significant reliability risk. These critical defects are often difficult to detect after the gate patterning step but can be more easily detected at the deposition steps. The detection at the deposition steps will not only increase the detection probability (capture rate of those critical defects) and will result in finding the defects closer to the defect source if caused by the deposition / clean steps and not the patterning process steps.

Biography

EDUCATION: Diplom Ing. (FH) Feinwerktechnik Fachhochschule München Germany

RANGE OF EXPERIENCE: 36 year's experience in the industry, working in product and application engineering for defect inspection, CD and overlay metrology. Management of highly experienced team of Yield Management Consultants and Product Managers in Europe. Special yield assignments at leading fabs in Europe, US and Asia.

PROFESSIONAL AND BUSINESS EXPERIENCE:

1982 - 1989 Karl Suss GmbH Munich Germany. Product development and application of production lithography tools for semiconductor industry.

1989 - 1995 KLA Instruments. Application engineer for Defect inspection, CD and Overlay Metrology in US and Europe.

1995 - 2003 KLA-Tencor Director Yield Management Consulting Europe. (Started Yield Management team in Europe)

2003 - 2008 Technical Director Southern Europe.

2008 - 9 month Yield / defect assignment at leading Fab in Asia.

2008 – 2011 Marketing Director Wafer Defect Inspection ICOS division.

2011 - 2013 Technical Director Europe for Defect and Metrology Products.

Since 2013 Senior Consultant in PCS (Process Control Solution) team at KLA-Tencor.

PUBLICATIONS & PATENTS:

- "Defect Density Monitor of Cluster Tools in the Photo Area", Semicon Europa 1996.
- "Defect Reduction and Yield Enhancement during a Fab Start Up" Productronica Munich 1997, Semicon Europa 1998.
- "Defect Reduction for 20nm High-k Metal Gate Technology" ASMC Saratoga Springs 2015
- Teacher @ ST University - Process Control
- PWQ Patent – EV205758708US

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (13:30-13:55hrs)

Speaker	Mr. Tim KRYMAN
Company	Rudolph Technologies Inc, USA
Designation	Senior Director, Corporate Marketing
Title of Presentation	**Laser-Based Inspection Technique for Non-Visual Defects**
Abstract	As Moore's law slows down, a transformation of the semiconductor industry is underway—advanced packaging is now an integral part of the scaling and functionality roadmaps. Through incorporating 2.5D, 3D and WLCSP (fan-in and fan-out technologies), manufacturers are able to preserve their edge on their circuits' shrink, reduce costs, improve performance, and maintain quality. Today's devices are expected to achieve zero-defect status. Traditional inspection techniques are not capable of uncovering non-visual defects that impact yield and downstream reliability. New inspection techniques are needed to ensure zero-defect. A new technique has been proven capable of detecting nanometer-level residues and residual metals after etch when current brightfield and darkfield inspection techniques lack the sensitivity.
Biography 	Tim Kryman is the senior director of corporate marketing at Rudolph focusing on product management and market development. Tim has been with Rudolph for over 17 years and has held positions in program management, customer support, strategic account management, and product management. Prior to Rudolph, Tim held a position as a marketing services manager at Ingersoll-Rand in their corporate marketing service group. Tim holds a BS in Accounting and Information Systems from Lock Haven University and an MBA from DeSales University.

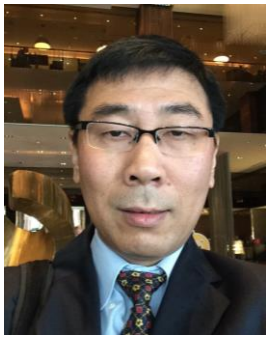
Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (13:55-14:20hrs)

Speaker	Dr. Martin KEIM
Company	Mentor, A Siemens Business, USA
Designation	Engineering Director & Product Marketing Manager
Title of Presentation	**How to Meet Extreme IoT Yield Demands on Mature Process Nodes with Volume Diagnosis and Statistical Yield Analysis**
Abstract	The Internet of Things (IOT) continues to deliver on its early promises of connected devices all around us. Although the devices are not the most advanced from a design or process technology point of view, they must be made in very high volume at very low cost and have short time to market. To deliver on the IOT promise, the industry relies on high yield performance from some of the most mature technology nodes. These are 200mm wafer fabs, 10-20 years old with process and metrology equipment that needs constant maintenance to run processes within control limits. Worldwide 200mm capacity is being fully utilized running at or near 100% capacity. 200mm equipment is not readily available in the marketplace to grow the capacity or build new fabs. So how do semiconductor manufacturers meet increasing demand? They must drive every fraction of a percent of yield from current factories. They must recover immediately from process excursions. They must predict process drift or excursions due to old equipment without any further capital investment in new process technology or increased metrology sampling. They must avoid product specific hidden yield limiters. This presentation will detail how adopting high volume diagnosis combined with automated statistical analysis provides a valuable tool to enable IOT product yields. This software-based volume diagnosis approach has been adopted by leading edge 300mm technology nodes for accelerating time to root cause driving rapid yield ramp. In the age of IoT, this software-based solution may provide even more value for mature technology nodes.
Biography 	Dr. Martin Keim joined the Silicon Test Solutions group of Mentor Graphics in 2001, now a Siemens Business, where he is currently Engineering Director of the Memory Built-In Self-Test and Silicon Insight team. He is a secretary of the IEEE P1687.1 working group and past member of the IEEE 1687 working group. He was editor of the sixth edition of the Microelectronics Failure Analysis Desk Reference Manual, responsible for the test and diagnosis chapters. He is currently editor of the EDFA magazine. For several years, Dr. Keim has worked on the organizing committee of the International Symposium for Testing and Failure Analysis, for which he was General Chair in 2016. He holds several national and international patents and is author of many technical publications. He received a doctorate in Informatics from the Albert-Ludwigs University in Germany.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (14:20-14:45hrs)

Speaker	Dr. Allen GU
Company	ZEISS Semiconductor Manufacturing Technology, USA
Designation	Staff Development Engineer
Title of Presentation	**High-Resolution 3D X-Ray Metrology for Semiconductor Packaging Development and Assembly**
Abstract	The 3D X-ray microscopic (XRM) imaging technique has become integrated in the electronics package failure analysis workflow because it can visualize buried defective regions without the need to destroy a specimen. In this paper we propose a new XRM application that enables a non-destructive metrology at unparalleled sub-micron resolution in three-dimension. Because the measurement is based on full-angle 3D tomography, it is possible to generate rich volumetric information on a variety of packaging structures that cannot be measured by the traditional cross-section technique. Additionally, the XRM based metrology has an advantage over the traditional coordinate measuring machines (CMM) technique because it can measure internal structures, which are not physically accessible by CMM probes. To the best of our knowledge, the 3D non-destructive metrology as shown here for the measurement of buried 3D interconnects in semiconductor packages at sub-micron resolution has not been reported previously. Several smartphone camera modules were used to develop and test this metrology workflow. The measurement focused on two major components in the camera module: CMOS imaging sensor (CIS) package and lens optics assembly. After the samples were imaged with XRM at high resolution, a measurement workflow followed to extract Au bump height, volume, surface area, and other critical dimensions in the CIS package. In the case of lens optics assembly, the measurements were the lens gap between multiple-layer stacks, lens thickness, lens tilt and de-centricity. The lens tilt and de-center measurements were obtained on both in-plane and out-of-plane orientations. A local adaptive surface determination algorithm was used to probe lens surface with sub-pixel accuracy and precision. The workflow was scripted to test multiple repetitive parts for high repeatability and reproducibility. Other 3D metrics may be developed with this metrology workflow. Due to the increasing complexity of emerging 3D packages, the packaging industry faces challenges for finding effective inspection and metrology techniques. The 3D X-ray metrology proposed in this paper offers a potential solution, because it uniquely enables non-destructive 3D metrology at submicron resolution.

Biography



Allen Gu spent his past over 17 years in a variety of microscopy technologies with a focus on micro/nanoscale imaging and analysis. He joined ZEISS X-ray Microscopy (formerly Xradia) in 2010 and played a leading role in the application development of world's most advanced 3D X-ray microscopy. Now the non-destructive technology that he helped to develop is a widely recognized brand for semiconductor package failure analysis. Recently, his work has been focused on driving the ZEISS product strategic roadmap for electronics market and developing new quantifiable near-line solutions for better quality control and assurance in package production. Now he looks for re-introducing and re-assembling most advanced 3D metrology techniques to semiconductor packaging industry.

Prior to his ZEISS career, Allen was a Senior Scientist and Applications Manager for scanning probe microscopy technology in Pacific Nanotechnology and Agilent, where he helped develop and market the technology for nano imaging and analysis.

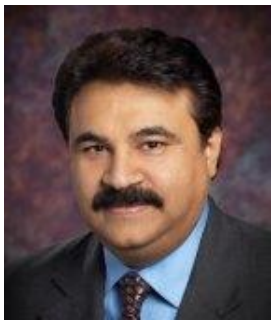
Allen's passion has been in material microstructural analysis and measurement since his Ph.D. thesis work. He studied a molecular self-assembly method to fabricate electrically conductive and magnetic nanowires and other nanostructures. Allen Gu was awarded Ph.D. degree by Louisiana Tech University, USA. He has authored 50+ articles in peer-reviewed journals, book chapter and conferences.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (15:10-15:35hrs)

Speaker	Dr. SHANG Yang
Company	Advantest (Singapore) Pte Ltd, Singapore
Designation	Senior Engineer
Title of Presentation	**3D Chip Defect Characterization by High Resolution Time-Domain Reflectometry**
Abstract	Recent years, the rapid growing of Internet of Things (IoT) and 4/5G technology has been continuously challenging the conventional IC packaging methods and functionalities. On one hand, higher I/O density is required to support more complex chip function and higher data through-put; on the other hand, larger I/O bandwidth is required for high speed data transfer up to mm-wave region (30~200GHz). Because of the greatly increased packaging complexity in the 2.5/3D realm, it becomes more challenging to analysis the failure of interconnections compared to that of the conventional packaging. Many non-destructive inspection tools such as X-ray and C-SAM have some limitations in efficiently finding out the defect of a 3D chip with sufficient resolution. As a result, more advanced inspection tools, such as a high resolution TDR system with electro-optic sampling technique is developed for rapid defect characterization and localization in a micron-meter (μm) resolution. Compared to the conventional oscilloscope based TDR, a high resolution TDR system has a greatly increased measurement bandwidth and resolution by utilizing ultra-short impulse signals originated from femtosecond laser source. In a high resolution TDR system, the reflected impulse waveforms in time domain will provide an intuitive understanding on the defect mode and locations when propagating in a uniform transmission-line (T-line) environment. However, the linear time-distance relationship of pulse signal could be distorted by the parasitic inductance and capacitance in the circuit network, leading to a false estimation of failure location in the chip packaging. In addition, low pass filtering (LPF) effect is almost everywhere due to the existence of lossy trace and substrate in the packaging. The LPF effect will broaden the incoming pulse and reduce the accuracy of pulse timing. In this presentation, the circuit network modeling technique will be discussed to accurately localize the failure point in the interconnection network based on the high resolution TDR analysis results for the characterization of various defects in 3D chips.
Biography	Dr. Yang Shang is currently at Advantest (Singapore), working on various applications of terahertz technology. After he obtained his honored B.S. degree in electrical and electronic engineering from Nanyang Technological University (NTU) in 2005, he spent more than 5 years' work on the measurement equipment and system design in the satellite communication industry, within which period he received his M.S. degree in 2009 from NTU. Then he was selected by the Joint Industry Postgraduate (JIP) Programme of Singapore Economic Development

	Board (EDB), spending 3 years in Virtus IC Design Centre of Excellence in NTU and obtained his Ph. D degree in February 2015, with major of terahertz integrated circuit design and applications. Dr. Yang Shang has 39 peer-reviewed and referred publications [conference (21), journal (15) book and chapters (2), patent (1)]. He was also the student paper competition finalists in IEEE SiRF'13 and RFIC'13, and received his best paper award at IEEE Singapore MTT/AP Chapter in 2014 and excellent patent award at ADVANTEST in 2015.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (15:35-16:00hrs)

Speaker	Mr. Ankush OBERAI & Ms. Rupa KAMOJI
Company	Synopsys Inc, USA & Synopsys India Pvt Ltd, India
Designation	Group Director, R&D & Senior Manager, R&D
Title of Presentation	**Fault Isolation of 2.5D and 3D Packages Through Analysis Across Entire System**
Abstract	The need to increase transistor packing density beyond Moore's Law and the need for expanding functionality, real-estate management and faster connections has pushed the industry to develop complex 2.5D and 3D package technology which includes System-in-Package (SiP), wafer-level packaging, through-silicon-vias (TSV), stacked-die packages. The high level of functional integration and the complex package architecture in these, pose a significant challenge for conventional Fault Isolation (FI) and Failure analysis (FA) methods. Various FA tools available the industry provide key data for the fault isolation in packages. Very often, one need to correlate the package level results from tool across the entire system for accurate fault isolation. This means, the results must be taken across the system and perform analysis at each level in the system. In this paper, we are presenting case studies for different methods to perform analysis across the system for accurate fault isolation.
Biography 	35 years in Semiconductor Industry, IC Design and Semiconductor Manufacturing. Serial Entrepreneurial and known for his success of Knights Technology Inc. Inventor of Industry Standard products: 1. Cad Navigation for Multiple Failure analysis tools 2. Yield Management for Semiconductor Fabs 3. Design Based solution for In-Fab Metrology manufacturing equipment Several US Patents granted for invention in above products. Started career as IC design and verification at NCA Corp in 1983. Later ventured out to realize his dream of becoming an inventor and entrepreneur by being part of a startup team which named the company as Knights Technology Inc. The company stated with Failure analysis software “Merlin” now the Industry standard product, owning 98% market share. In 1995, invented Yield Management product, which brought a new wave of manufacturing improvement in productivity and cost savings. In 2012, Knights merged with Synopsys. Knights products continues to grow and maintains market leadership.

	Working in the software development of CAD Navigation products used for Failure Analysis of IC Chips and SoCs / Packages / PC Boards for 18 years. Started career with Knights Technology Inc. which is now part of Synopsys Inc. Cad Navigation products are designed to read in various design data, provides various advanced debug utilities for accurate and faster fault isolation and faster root cause analysis of IC chips and Packages. The software also interfaces with multiple Failure Analysis equipment and help FA engineer to drive the equipment to area of interest for localized analysis. Specialized in various design formats, manages design of software features to meet needs of advanced Failure Analysis flows of IC chips designed and manufactured with lower technology nodes.

Topics and Abstracts: IC Failure Analysis & Defects Characterisation Forum (16:00-16:25hrs)

Speaker	Dr. Suhairi SAHARUDIN
Company	MIMOS Semiconductor (M) Sdn Bhd, Malaysia
Designation	Senior Staff Researcher
Title of Presentation	**Probing and Measurement of Material Properties Using Advanced Surface Characterization Tools for Successful Failure Analysis Investigations**
Abstract	Failure analysis involves mechanical, physical, and chemical investigation into the cause and sequence of events that lead to a product condition in which the product no longer meets expectations. Material investigation for identification and verification of materials compliment other traditional failure analysis techniques such as microscopy and physical analysis. Among the important material investigation tools in failure analysis involves technique such as spectroscopy and X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES) and Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS). Together with advancement in physical analysis equipment such as in High Resolution Transmission electron microscopy (HRTEM) and Dual-Beam Focused Ion Beam-Scanning Electron Microscope systems (FIB-SEMs), effective probing and measurement of failure in various application are made possible by combining advancement in both material and physical analytical techniques. Analysis techniques of such tools are described in this talk with brief introduction of its principles of operation and application towards failure analysis through use of several case studies.
Biography 	The speaker obtained his basic degree in Electrical and Electronics Engineering from University of Stratchlyde, Glasgow, Scotland. Following his interest in emerging technologies back then in lasers and fiber optics, he further pursued his Masters degree in Optical Electronics in 1992 and established his career path in this field for the following 20 years as researcher in SIRIM Berhad and MIMOS Berhad (present). He concluded his academic endeavor in the same field of interest (Photonics) through Doctoral degree in Fiber laser research in 2006 from Universiti Putra Malaysia. He was among the founder of IEEE Photonics Society Malaysian chapter (previously known as IEEE Laser and Electro-optic society) and actively involved as Secretary and Chairman of the society. His 20 years of R&D experience and skills is now being directed towards activities involving technical problem identification such as Failure Analysis process. He currently is establishing a new interest in spectroscopic methods in failure analysis process particularly in Surface Analysis field.