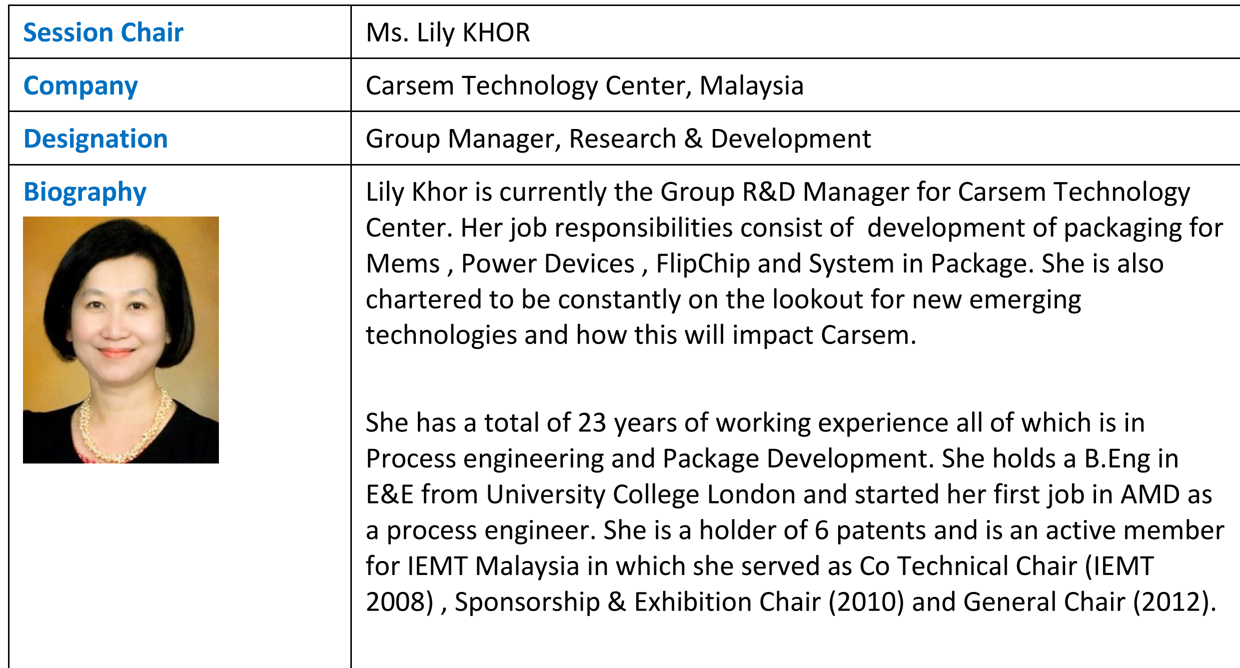
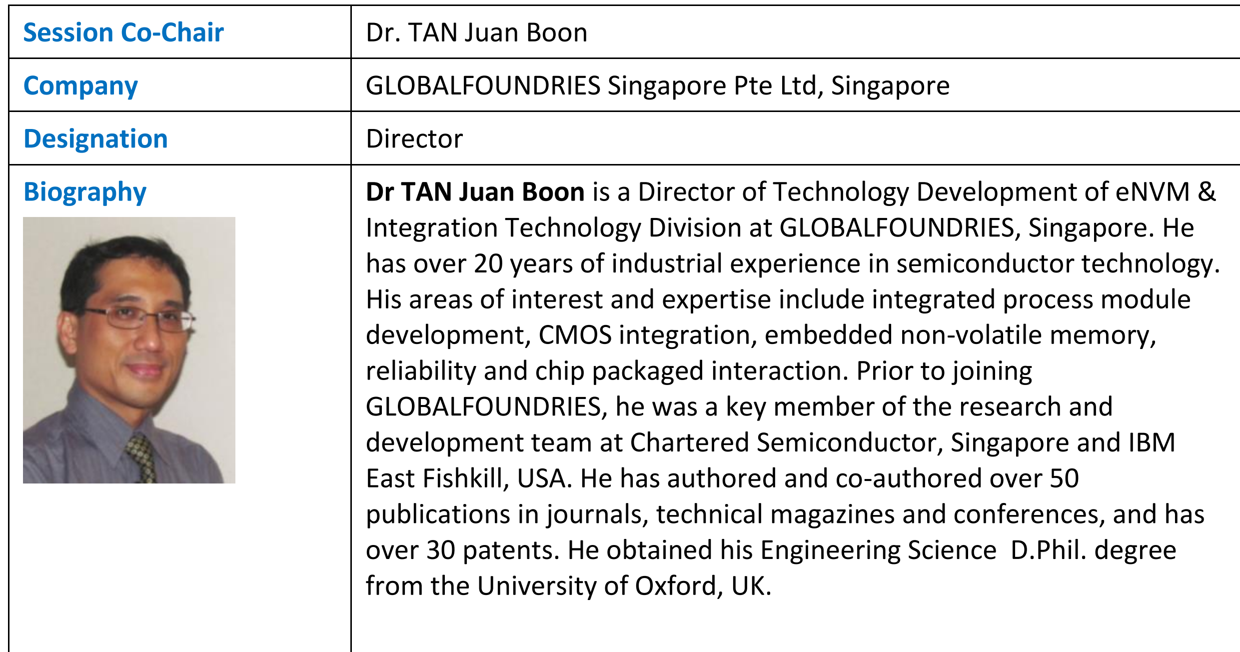
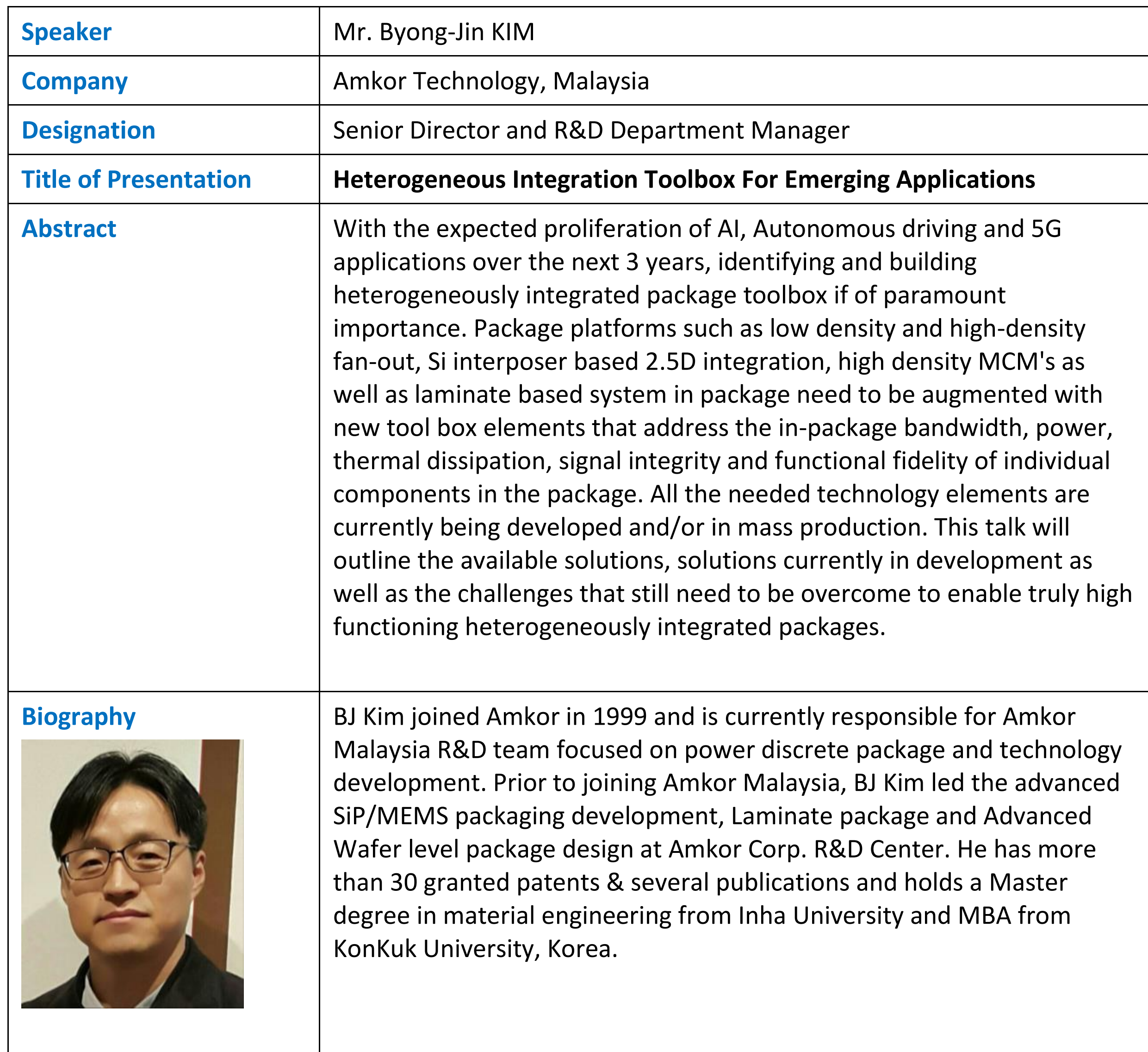
# Topics and Abstracts: Advanced Packaging Forum (Chairperson)

| Session Chair | Ms. Lily KHOR |
|---|---|
| Company | Carsem Technology Center, Malaysia |
| Designation | Group Manager, Research & Development |
| Biography  | Lily Khor is currently the Group R&D Manager for Carsem Technology Center. Her job responsibilities consist of development of packaging for Mems , Power Devices , FlipChip and System in Package. She is also chartered to be constantly on the lookout for new emerging technologies and how this will impact Carsem.<br><br>She has a total of 23 years of working experience all of which is in Process engineering and Package Development. She holds a B.Eng in E&E from University College London and started her first job in AMD as a process engineer. She is a holder of 6 patents and is an active member for IEMT Malaysia in which she served as Co Technical Chair (IEMT 2008) , Sponsorship & Exhibition Chair (2010) and General Chair (2012). |

# Topics and Abstracts: Advanced Packaging Forum
# (Co-Chairperson)

| **Session Co-Chair** | Dr. TAN Juan Boon |
|---|---|
| **Company** | GLOBALFOUNDRIES Singapore Pte Ltd, Singapore |
| **Designation** | Director |
| **Biography**  | **Dr TAN Juan Boon** is a Director of Technology Development of eNVM & Integration Technology Division at GLOBALFOUNDRIES, Singapore. He has over 20 years of industrial experience in semiconductor technology. His areas of interest and expertise include integrated process module development, CMOS integration, embedded non-volatile memory, reliability and chip packaged interaction. Prior to joining GLOBALFOUNDRIES, he was a key member of the research and development team at Chartered Semiconductor, Singapore and IBM East Fishkill, USA. He has authored and co-authored over 50 publications in journals, technical magazines and conferences, and has over 30 patents. He obtained his Engineering Science D.Phil. degree from the University of Oxford, UK. |

# Topics and Abstracts: Advanced Packaging Forum (09:35-10:00hrs)



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| **Speaker** | Mr. Byong-Jin KIM |
| **Company** | Amkor Technology, Malaysia |
| **Designation** | Senior Director and R&D Department Manager |
| **Title of Presentation** | **Heterogeneous Integration Toolbox For Emerging Applications** |
| **Abstract** | With the expected proliferation of AI, Autonomous driving and 5G applications over the next 3 years, identifying and building heterogeneously integrated package toolbox if of paramount importance. Package platforms such as low density and high-density fan-out, Si interposer based 2.5D integration, high density MCM's as well as laminate based system in package need to be augmented with new tool box elements that address the in-package bandwidth, power, thermal dissipation, signal integrity and functional fidelity of individual components in the package. All the needed technology elements are currently being developed and/or in mass production. This talk will outline the available solutions, solutions currently in development as well as the challenges that still need to be overcome to enable truly high functioning heterogeneously integrated packages. |
| **Biography** | BJ Kim joined Amkor in 1999 and is currently responsible for Amkor Malaysia R&D team focused on power discrete package and technology development. Prior to joining Amkor Malaysia, BJ Kim led the advanced SiP/MEMS packaging development, Laminate package and Advanced Wafer level package design at Amkor Corp. R&D Center. He has more than 30 granted patents & several publications and holds a Master degree in material engineering from Inha University and MBA from KonKuk University, Korea. |

# Topics and Abstracts: Advanced Packaging Forum (10:00-10:25hrs)

| **Speaker** | Mr. LEE Chee Ping |
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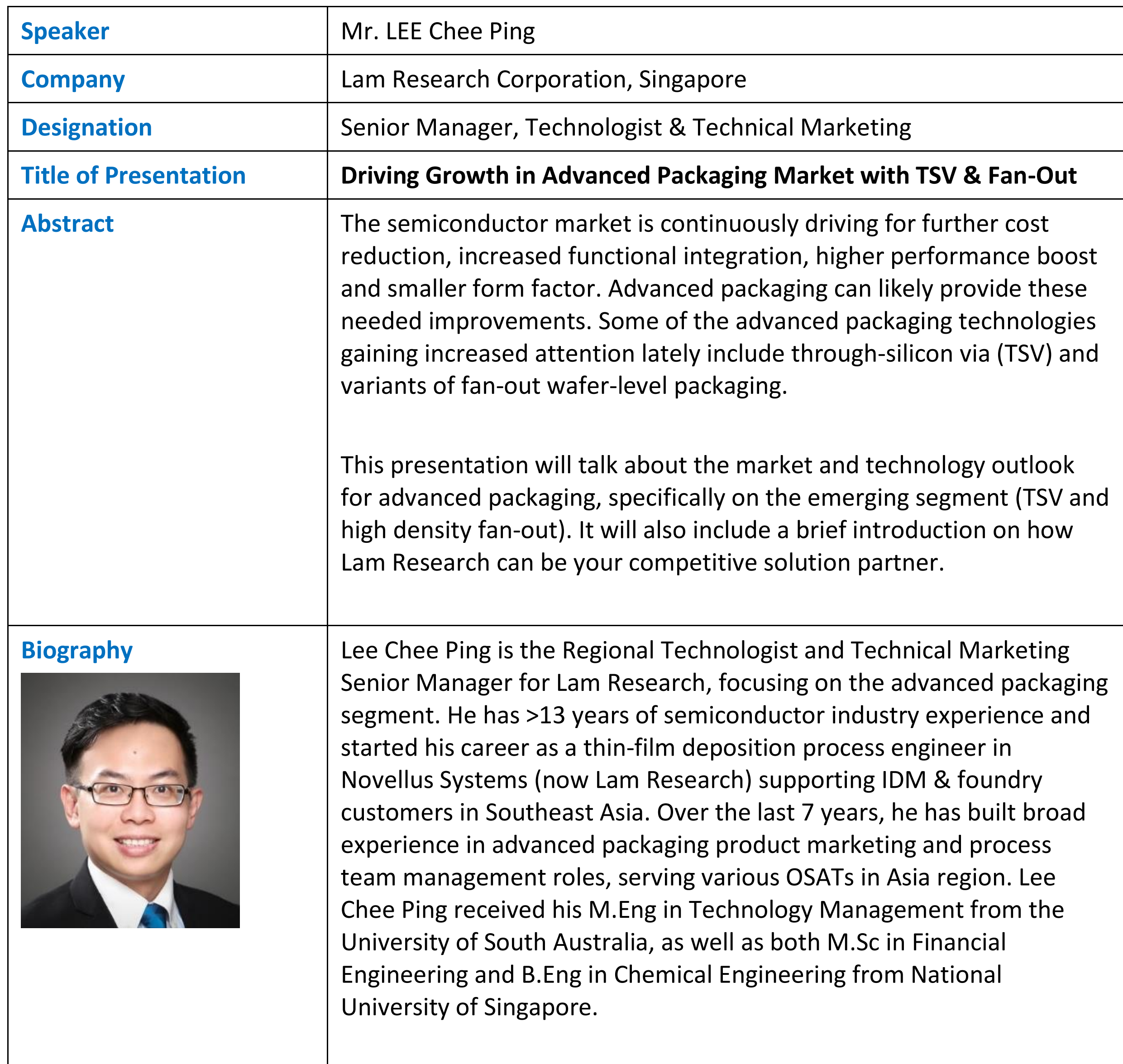
| **Company** | Lam Research Corporation, Singapore |
| **Designation** | Senior Manager, Technologist & Technical Marketing |
| **Title of Presentation** | **Driving Growth in Advanced Packaging Market with TSV & Fan-Out** |
| **Abstract** | The semiconductor market is continuously driving for further cost reduction, increased functional integration, higher performance boost and smaller form factor. Advanced packaging can likely provide these needed improvements. Some of the advanced packaging technologies gaining increased attention lately include through-silicon via (TSV) and variants of fan-out wafer-level packaging.<br><br>This presentation will talk about the market and technology outlook for advanced packaging, specifically on the emerging segment (TSV and high density fan-out). It will also include a brief introduction on how Lam Research can be your competitive solution partner. |
| **Biography**<br> | Lee Chee Ping is the Regional Technologist and Technical Marketing Senior Manager for Lam Research, focusing on the advanced packaging segment. He has >13 years of semiconductor industry experience and started his career as a thin-film deposition process engineer in Novellus Systems (now Lam Research) supporting IDM & foundry customers in Southeast Asia. Over the last 7 years, he has built broad experience in advanced packaging product marketing and process team management roles, serving various OSATs in Asia region. Lee Chee Ping received his M.Eng in Technology Management from the University of South Australia, as well as both M.Sc in Financial Engineering and B.Eng in Chemical Engineering from National University of Singapore. |

# Topics and Abstracts: Advanced Packaging Forum (10:25-10:50hrs)

| Speaker | Mr. Henry LIN |
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| Company | ASE Group, Taiwan |
| Designation | Manager, Embedded Design Team |
| Title of Presentation | **Embedded Solution for Next Generation Application** |
| Abstract | TBA |
| Biography | Henry Lin is the manager with embedded product design.<br>He currently focuses on embedded die packaging and has good experience in module development.<br>He received his MSc degree in microwave engineering from University of Surrey, UK in 2006. |

# Topics and Abstracts: Advanced Packaging Forum (10:50-11:15hrs)

| Speaker | Dr. Takenori FUJIWARA |
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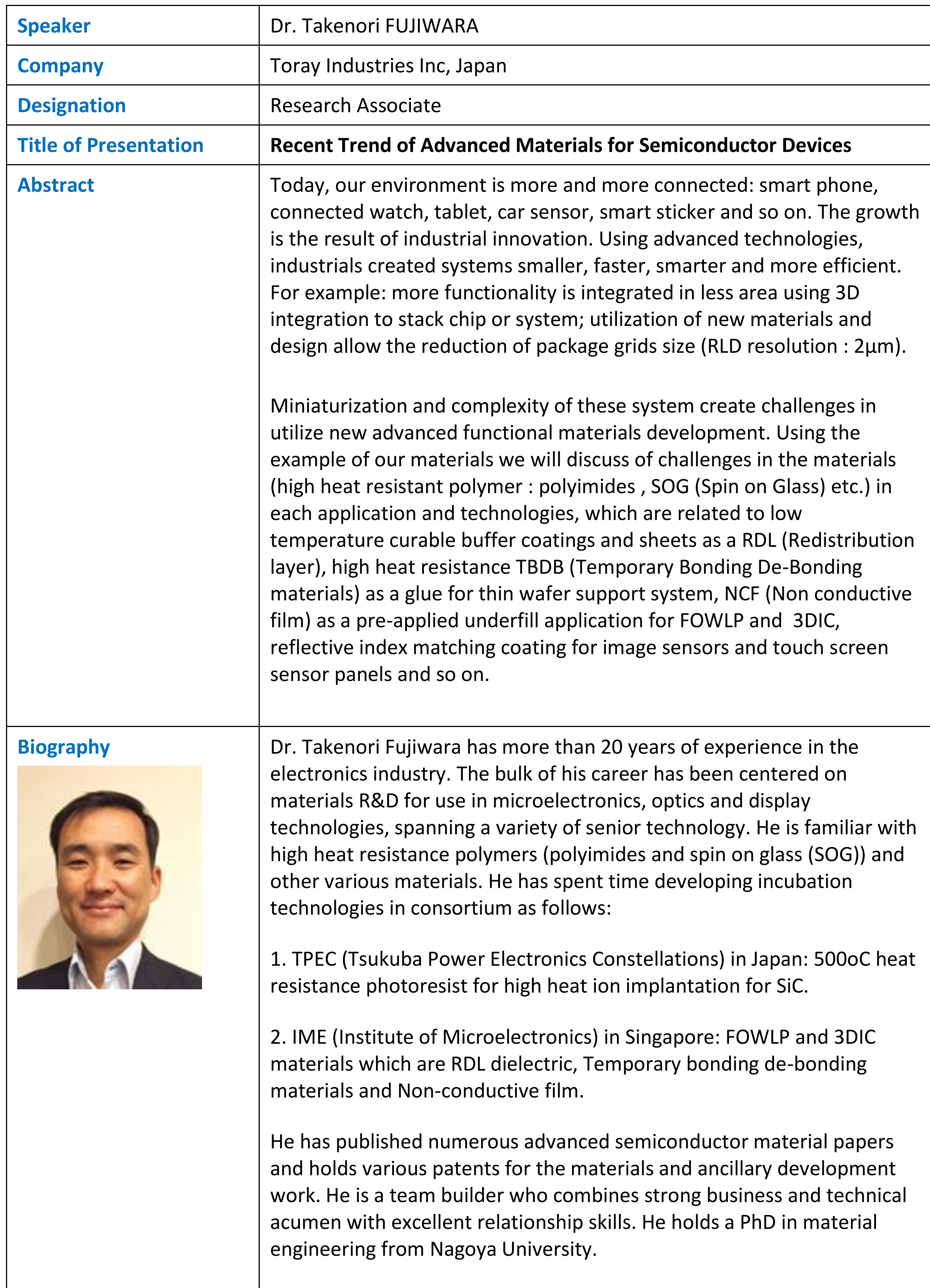
| Company | Toray Industries Inc, Japan |
| Designation | Research Associate |
| Title of Presentation | **Recent Trend of Advanced Materials for Semiconductor Devices** |
| Abstract | Today, our environment is more and more connected: smart phone, connected watch, tablet, car sensor, smart sticker and so on. The growth is the result of industrial innovation. Using advanced technologies, industrials created systems smaller, faster, smarter and more efficient. For example: more functionality is integrated in less area using 3D integration to stack chip or system; utilization of new materials and design allow the reduction of package grids size (RLD resolution : 2µm).<br><br>Miniaturization and complexity of these system create challenges in utilize new advanced functional materials development. Using the example of our materials we will discuss of challenges in the materials (high heat resistant polymer : polyimides , SOG (Spin on Glass) etc.) in each application and technologies, which are related to low temperature curable buffer coatings and sheets as a RDL (Redistribution layer), high heat resistance TBDB (Temporary Bonding De-Bonding materials) as a glue for thin wafer support system, NCF (Non conductive film) as a pre-applied underfill application for FOWLP and 3DIC, reflective index matching coating for image sensors and touch screen sensor panels and so on. |
| Biography  | Dr. Takenori Fujiwara has more than 20 years of experience in the electronics industry. The bulk of his career has been centered on materials R&D for use in microelectronics, optics and display technologies, spanning a variety of senior technology. He is familiar with high heat resistance polymers (polyimides and spin on glass (SOG)) and other various materials. He has spent time developing incubation technologies in consortium as follows:<br><br>1. TPEC (Tsukuba Power Electronics Constellations) in Japan: 500oC heat resistance photoresist for high heat ion implantation for SiC.<br><br>2. IME (Institute of Microelectronics) in Singapore: FOWLP and 3DIC materials which are RDL dielectric, Temporary bonding de-bonding materials and Non-conductive film.<br><br>He has published numerous advanced semiconductor material papers and holds various patents for the materials and ancillary development work. He is a team builder who combines strong business and technical acumen with excellent relationship skills. He holds a PhD in material engineering from Nagoya University. |

# Topics and Abstracts: Advanced Packaging Forum (11:30-11:55hrs)

| Speaker | Mr. CHONG Chan Pin |
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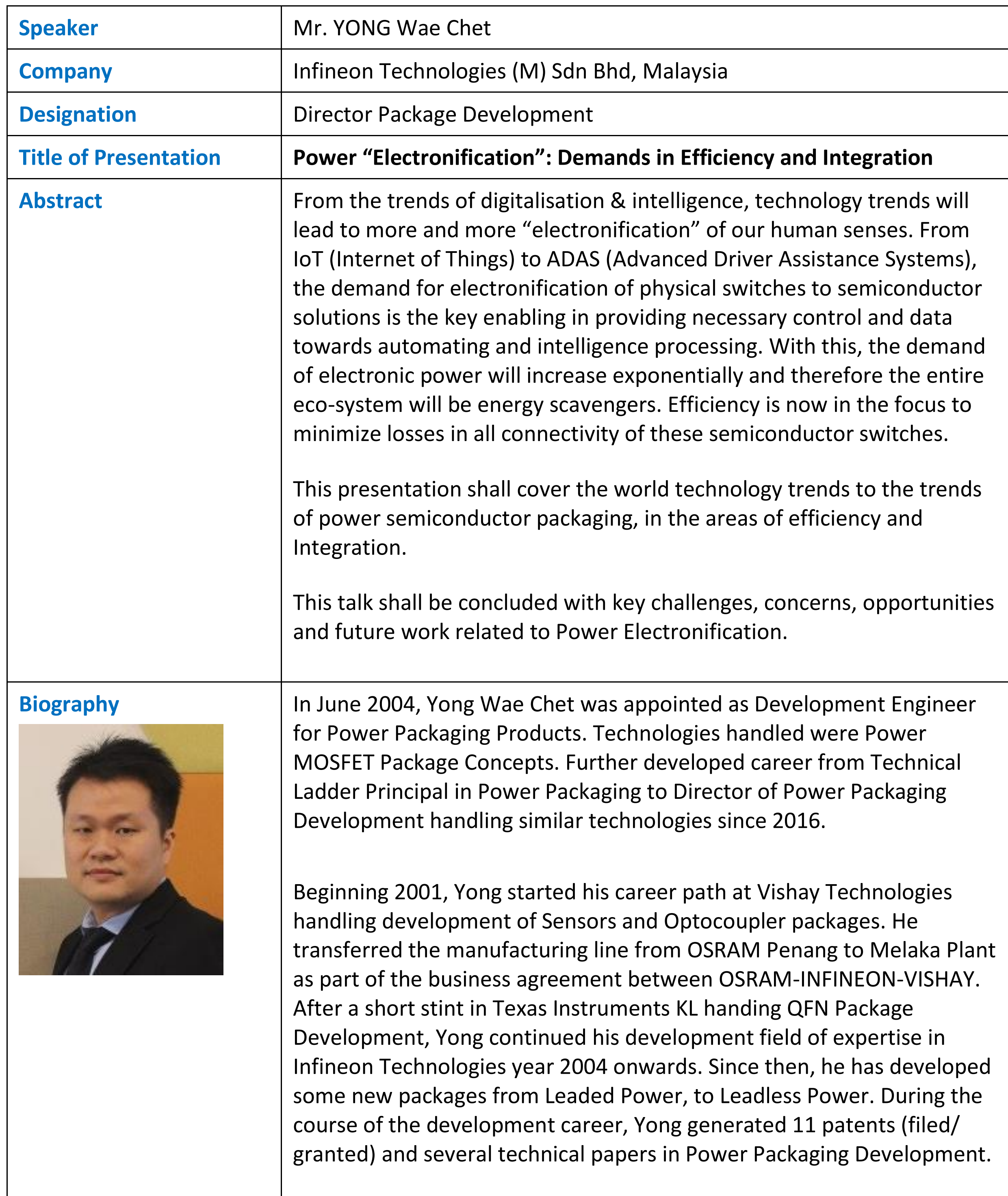
| Company | Kulicke & Soffa Pte Ltd, Singapore |
| Designation | Senior Vice President, EA/APMR and Wedge Bonders Business Units |
| Title of Presentation | **The ‘SMART-er’ Approach to Electronics Packaging** |
| Abstract | What is Advanced Packaging Solution? Year after year, we ask the same question and every year we come up with new answer. With the constant change in requirement, this year I would like to explore Advanced Packaging “SMART Electronics” need for integrating multiple functional dies like MEMs, sensors, RF, memory, ASIC etc in a single package. With greater use of Multichip Packages, System in Packages and Embedded die, there are greater need for SMART system to support these electronics. Let us explore some of these challenges and the technologies required to support this demand. |
| Biography | Chan Pin was most recently appointed as Senior Vice President of K&S’ EA/APMR and Wedge Bonders Business Units. He joined K&S in 2014 as Vice President of Wedge Bonders business group. Chan Pin had successfully turnaround the business and led the team to higher growth by diversifying the business into the battery bonding market.<br><br>Chan Pin is a technology industry veteran with more than 24 years of engineering and operations experience in the semiconductor and electronics industry. He started his career first as a Process and Test Engineer at Motorola Pagers and Cellular group and pioneered multiple factories in Asia before advancing to the role of Manufacturing Manager at Flextronics. In 1999, Chan Pin joined KLA-Tencor and held a number of diverse positions, including Senior Technical Director of Engineering and General Manager of Strategic Business Unit in Greater China. Chan Pin then pioneered the efforts of starting the MEMS factory in Singapore when he became the Vice President of Sales and General Manager at Form Factor. Most recently, he was the Global President & CEO at Everett Charles Technologies, managing and leading in test and probe technologies.<br><br>Chan Pin received his bachelor's degree in Electrical Engineering and Computer Science from the State University of New York at Buffalo and a master's degree in Business Administration from the University of Leicester, United Kingdom. A Singaporean national, he is a military reserve (National Service, NS) Brigade 2nd in Command of a combined arms division. |

# Topics and Abstracts: Advanced Packaging Forum (13:35-14:00hrs)



| Speaker | Mr. YONG Wae Chet |
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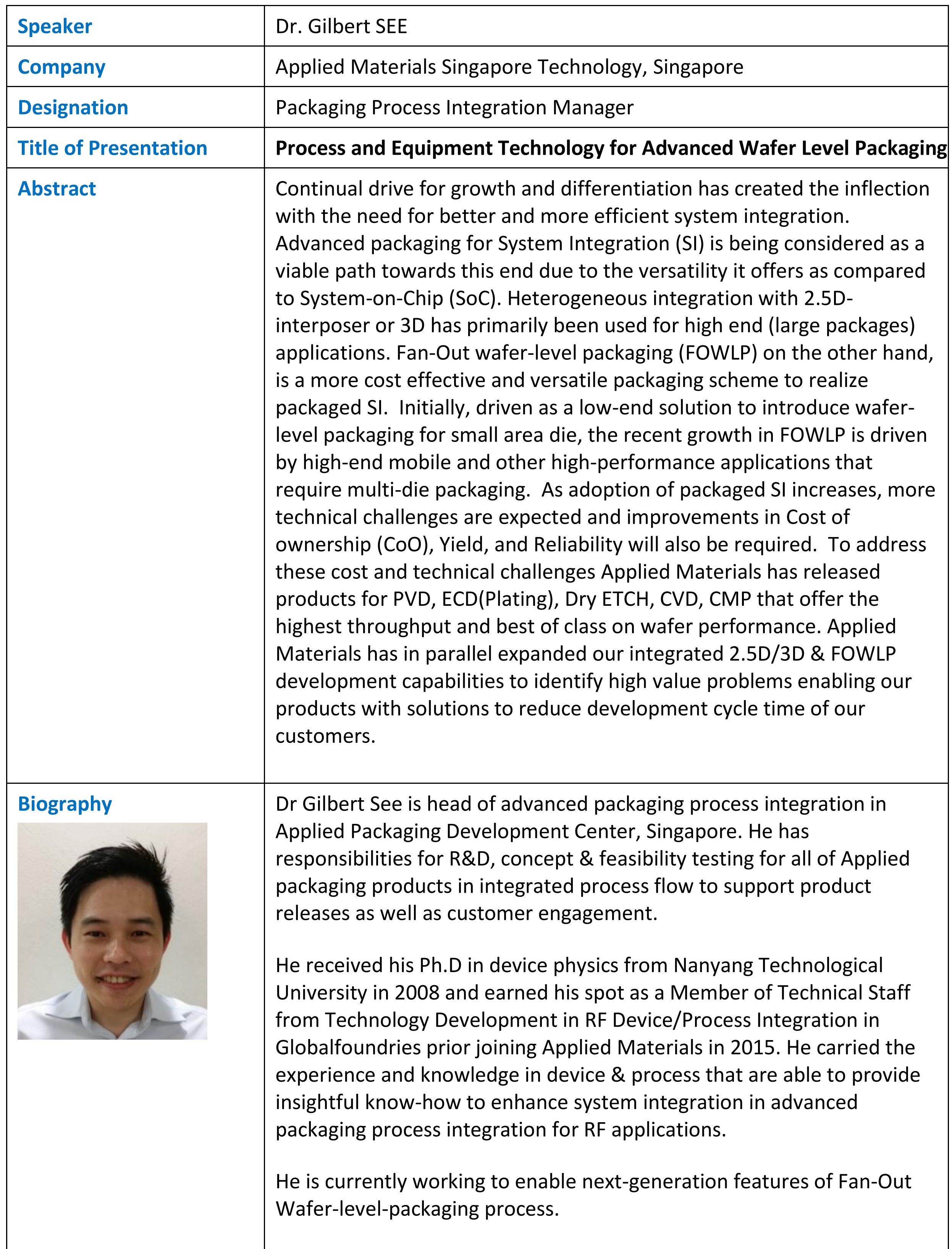
| Company | Infineon Technologies (M) Sdn Bhd, Malaysia |
| Designation | Director Package Development |
| Title of Presentation | **Power "Electronification": Demands in Efficiency and Integration** |
| Abstract | From the trends of digitalisation & intelligence, technology trends will lead to more and more "electronification" of our human senses. From IoT (Internet of Things) to ADAS (Advanced Driver Assistance Systems), the demand for electronification of physical switches to semiconductor solutions is the key enabling in providing necessary control and data towards automating and intelligence processing. With this, the demand of electronic power will increase exponentially and therefore the entire eco-system will be energy scavengers. Efficiency is now in the focus to minimize losses in all connectivity of these semiconductor switches.<br><br>This presentation shall cover the world technology trends to the trends of power semiconductor packaging, in the areas of efficiency and Integration.<br><br>This talk shall be concluded with key challenges, concerns, opportunities and future work related to Power Electronification. |
| Biography | In June 2004, Yong Wae Chet was appointed as Development Engineer for Power Packaging Products. Technologies handled were Power MOSFET Package Concepts. Further developed career from Technical Ladder Principal in Power Packaging to Director of Power Packaging Development handling similar technologies since 2016.<br><br>Beginning 2001, Yong started his career path at Vishay Technologies handling development of Sensors and Optocoupler packages. He transferred the manufacturing line from OSRAM Penang to Melaka Plant as part of the business agreement between OSRAM-INFINEON-VISHAY. After a short stint in Texas Instruments KL handing QFN Package Development, Yong continued his development field of expertise in Infineon Technologies year 2004 onwards. Since then, he has developed some new packages from Leaded Power, to Leadless Power. During the course of the development career, Yong generated 11 patents (filed/ granted) and several technical papers in Power Packaging Development. |

# Topics and Abstracts: Advanced Packaging Forum (14:00-14:25hrs)



| Speaker | Dr. Gilbert SEE |
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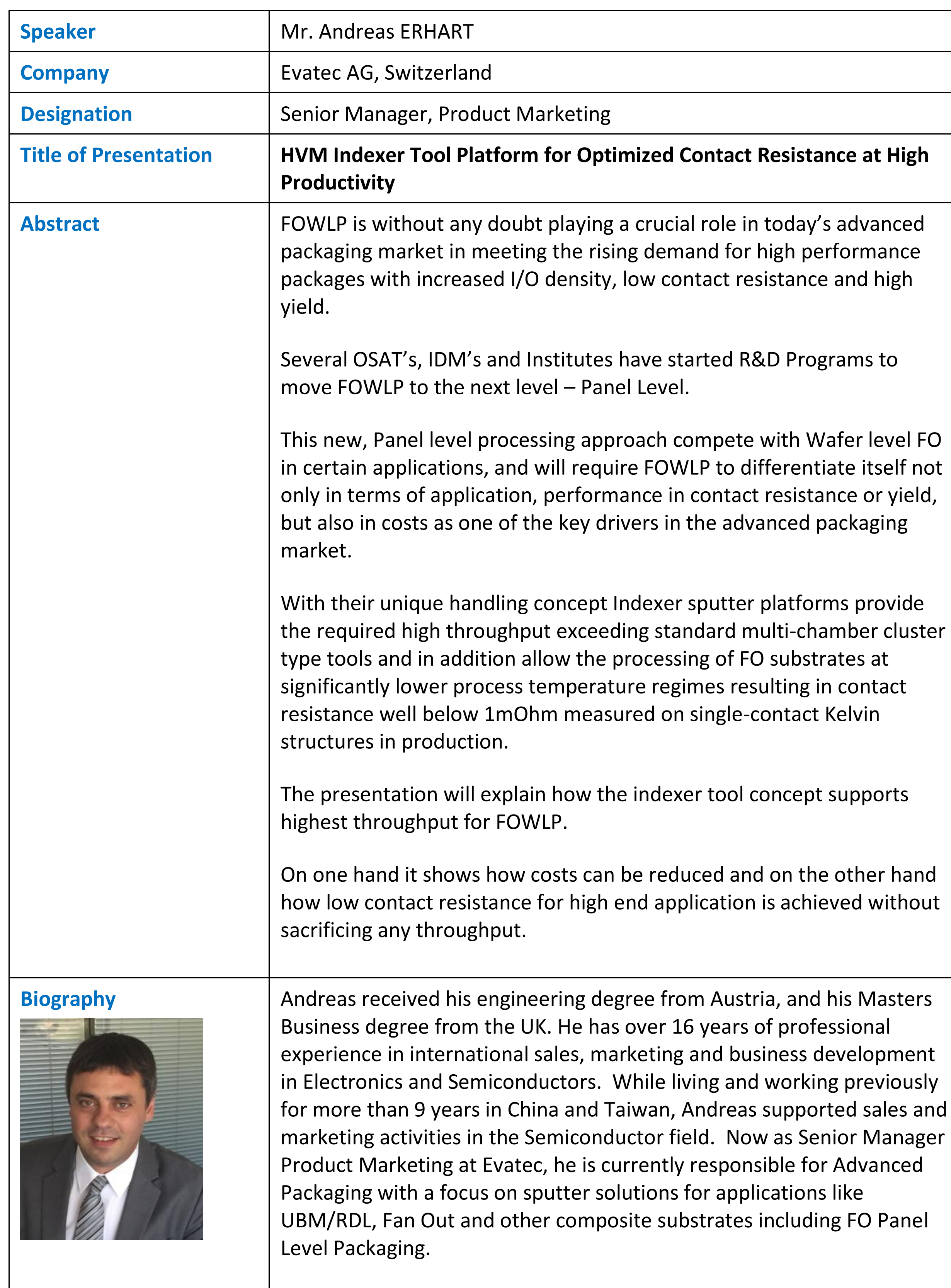
| Company | Applied Materials Singapore Technology, Singapore |
| Designation | Packaging Process Integration Manager |
| Title of Presentation | **Process and Equipment Technology for Advanced Wafer Level Packaging** |
| Abstract | Continual drive for growth and differentiation has created the inflection with the need for better and more efficient system integration. Advanced packaging for System Integration (SI) is being considered as a viable path towards this end due to the versatility it offers as compared to System-on-Chip (SoC). Heterogeneous integration with 2.5D-interposer or 3D has primarily been used for high end (large packages) applications. Fan-Out wafer-level packaging (FOWLP) on the other hand, is a more cost effective and versatile packaging scheme to realize packaged SI. Initially, driven as a low-end solution to introduce wafer-level packaging for small area die, the recent growth in FOWLP is driven by high-end mobile and other high-performance applications that require multi-die packaging. As adoption of packaged SI increases, more technical challenges are expected and improvements in Cost of ownership (CoO), Yield, and Reliability will also be required. To address these cost and technical challenges Applied Materials has released products for PVD, ECD(Plating), Dry ETCH, CVD, CMP that offer the highest throughput and best of class on wafer performance. Applied Materials has in parallel expanded our integrated 2.5D/3D & FOWLP development capabilities to identify high value problems enabling our products with solutions to reduce development cycle time of our customers. |
| Biography | Dr Gilbert See is head of advanced packaging process integration in Applied Packaging Development Center, Singapore. He has responsibilities for R&D, concept & feasibility testing for all of Applied packaging products in integrated process flow to support product releases as well as customer engagement.<br><br>He received his Ph.D in device physics from Nanyang Technological University in 2008 and earned his spot as a Member of Technical Staff from Technology Development in RF Device/Process Integration in Globalfoundries prior joining Applied Materials in 2015. He carried the experience and knowledge in device & process that are able to provide insightful know-how to enhance system integration in advanced packaging process integration for RF applications.<br><br>He is currently working to enable next-generation features of Fan-Out Wafer-level-packaging process. |

# Topics and Abstracts: Advanced Packaging Forum (14:25-14:50hrs)



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| **Speaker** | Mr. Andreas ERHART |
| **Company** | Evatec AG, Switzerland |
| **Designation** | Senior Manager, Product Marketing |
| **Title of Presentation** | **HVM Indexer Tool Platform for Optimized Contact Resistance at High Productivity** |
| **Abstract** | FOWLP is without any doubt playing a crucial role in today's advanced packaging market in meeting the rising demand for high performance packages with increased I/O density, low contact resistance and high yield.<br><br>Several OSAT's, IDM's and Institutes have started R&D Programs to move FOWLP to the next level – Panel Level.<br><br>This new, Panel level processing approach compete with Wafer level FO in certain applications, and will require FOWLP to differentiate itself not only in terms of application, performance in contact resistance or yield, but also in costs as one of the key drivers in the advanced packaging market.<br><br>With their unique handling concept Indexer sputter platforms provide the required high throughput exceeding standard multi-chamber cluster type tools and in addition allow the processing of FO substrates at significantly lower process temperature regimes resulting in contact resistance well below 1mOhm measured on single-contact Kelvin structures in production.<br><br>The presentation will explain how the indexer tool concept supports highest throughput for FOWLP.<br><br>On one hand it shows how costs can be reduced and on the other hand how low contact resistance for high end application is achieved without sacrificing any throughput. |
| **Biography** | Andreas received his engineering degree from Austria, and his Masters Business degree from the UK. He has over 16 years of professional experience in international sales, marketing and business development in Electronics and Semiconductors. While living and working previously for more than 9 years in China and Taiwan, Andreas supported sales and marketing activities in the Semiconductor field. Now as Senior Manager Product Marketing at Evatec, he is currently responsible for Advanced Packaging with a focus on sputter solutions for applications like UBM/RDL, Fan Out and other composite substrates including FO Panel Level Packaging. |

# Topics and Abstracts: Advanced Packaging Forum (15:05-15:30hrs)

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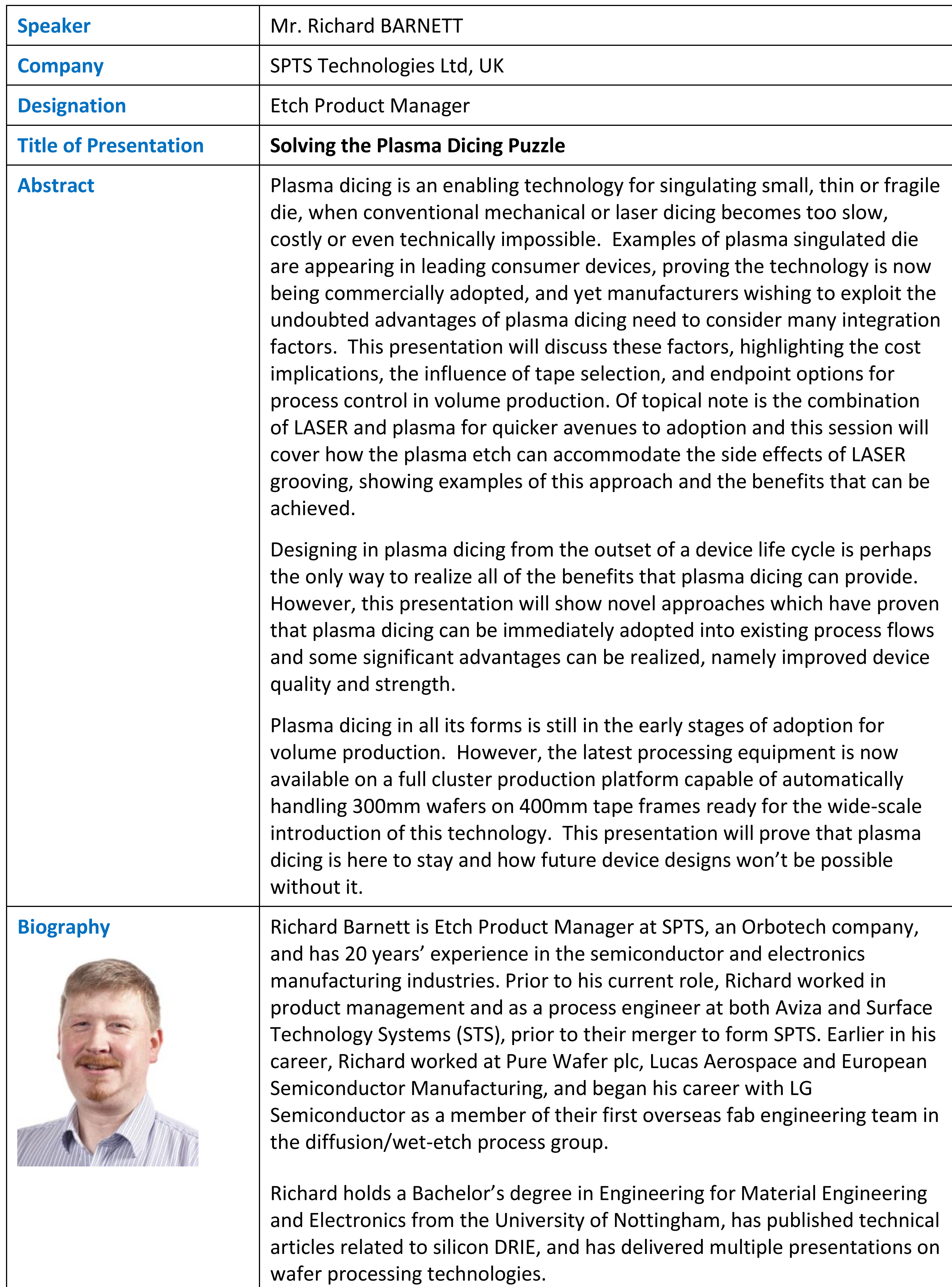
| **Speaker** | Mr. Richard BARNETT |
| **Company** | SPTS Technologies Ltd, UK |
| **Designation** | Etch Product Manager |
| **Title of Presentation** | **Solving the Plasma Dicing Puzzle** |
| **Abstract** | Plasma dicing is an enabling technology for singulating small, thin or fragile die, when conventional mechanical or laser dicing becomes too slow, costly or even technically impossible. Examples of plasma singulated die are appearing in leading consumer devices, proving the technology is now being commercially adopted, and yet manufacturers wishing to exploit the undoubted advantages of plasma dicing need to consider many integration factors. This presentation will discuss these factors, highlighting the cost implications, the influence of tape selection, and endpoint options for process control in volume production. Of topical note is the combination of LASER and plasma for quicker avenues to adoption and this session will cover how the plasma etch can accommodate the side effects of LASER grooving, showing examples of this approach and the benefits that can be achieved.<br><br>Designing in plasma dicing from the outset of a device life cycle is perhaps the only way to realize all of the benefits that plasma dicing can provide. However, this presentation will show novel approaches which have proven that plasma dicing can be immediately adopted into existing process flows and some significant advantages can be realized, namely improved device quality and strength.<br><br>Plasma dicing in all its forms is still in the early stages of adoption for volume production. However, the latest processing equipment is now available on a full cluster production platform capable of automatically handling 300mm wafers on 400mm tape frames ready for the wide-scale introduction of this technology. This presentation will prove that plasma dicing is here to stay and how future device designs won't be possible without it. |
| **Biography**  | Richard Barnett is Etch Product Manager at SPTS, an Orbotech company, and has 20 years' experience in the semiconductor and electronics manufacturing industries. Prior to his current role, Richard worked in product management and as a process engineer at both Aviza and Surface Technology Systems (STS), prior to their merger to form SPTS. Earlier in his career, Richard worked at Pure Wafer plc, Lucas Aerospace and European Semiconductor Manufacturing, and began his career with LG Semiconductor as a member of their first overseas fab engineering team in the diffusion/wet-etch process group.<br><br>Richard holds a Bachelor's degree in Engineering for Material Engineering and Electronics from the University of Nottingham, has published technical articles related to silicon DRIE, and has delivered multiple presentations on wafer processing technologies. |

# Topics and Abstracts: Advanced Packaging Forum
# (15:30-15:55hrs)

| Speaker | Mr. YU Xiang |
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| Company | Air Products and Chemicals (China) Investment Co Ltd, China |
| Designation | Gas Application Manager, Technical Application in Electronic Packaging and Assembly |
| Title of Presentation | **Production-Scale Flux-Free Wafer Bump Reflow by Activated Hydrogen** |
| Abstract | Packaging technology for electronics devices has advanced rapidly in recent years driven by feature size reduction, new materials developed, and increased demand on device functionality. The most fundamental among the advanced packaging technology is the use of wafer bumping and wafer-level chip scale packaging.<br><br>In a wafer bumping process, fine-pitch electroplated solder bumps are formed over an entire silicon wafer on which integrated circuits have been built, the wafer is then reflowed at a temperature above the solder's melting point to complete metallic interconnection of the bumps with underneath metal pads and convert the bumps from a deposited shape into a ball shape. After the wafer bumping, the wafer is cut into individual chips and goes through subsequent packaging processes. In the packed devices, the formed bumps serve as electrical, mechanical, and mounting connections. Current study is related to the last step of the wafer bumping process — wafer bump reflow.<br><br>This presentation will introduce a recent work by a joint effort between Air Products and Sikama International on developing and testing an EA-enabled prototype furnace for production-scale wafer bump reflow. Additional trial results and customer evaluations will be introduced in the presentation.<br><br>Comparing with the flux-containing and other flux-free processes, the EA-based technology offers the following benefits for wafer bump reflow:<br><br>1) enhanced bump reflow quality because the flux induced solder voids and wafer contaminations naturally disappear<br>2) improved productivity by having in-line process capability, eliminating post wafer cleaning, and avoiding furnace down time<br>3) reduced cost of ownership to end users due to eliminated costs associated with cleaning equipment, cleaning solution, labor work, and flux<br>4) improved safety by eliminating flux exposure and using a non-toxic and non-flammable gas mixture<br>5) no environmental issues by eliminating organic vapors, hazard residues, and CO2 emission. |

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<td>Biography<br> </td>
<td>Xiang Yu is a gas application manager for the electronic industry of Air Products and Chemicals (China) Investment Co., Ltd. He is responsible for the application technology development and operation in support of the advanced silicon and assembly process technology development as well as the manufacturing and product fault diagnostics. He works with the industry to drive synergistic collaboration and development to advance process and diagnostic capability for the semiconductor industry. Xiang holds three patents, primarily in the field of advanced IC packaging technology development engineering, and has successfully developed WLCSP and POP product use for cell phone chip processer, fan-out product for SSD controller and the side wall which is high band width and high capacity product for NAND-flash.<br><br>Xiang is a partner in the development of the novel flux-free technology that is introduced in the paper. This technology has a good potential to be widely used for electronics packaging and has received increasing interests from key customers. In the presentation, Xiang is going to introduce a recent work by a joint effort between Air Products and Sikama on developing and testing a production-scale unit for the novel flux-free technology for wafer bump reflow.</td>
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# Topics and Abstracts: Advanced Packaging Forum (15:55-16:20hrs)

| Speaker | Ms. LIM Sze Pei |
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| Company | Indium Corporation, Malaysia |
| Designation | Regional Product Manager, Semiconductor |
| Title of Presentation | **Challenges in Material Selection for SIP Applications** |
| Abstract | The recent surge in demand for system-in-package (SiP) applications is driven by the rapid development of connected “smart” devices. The versatility and capability of heterogeneous integration for SiP have made it a popular choice of packaging solutions for increased functionality in a smaller package form factor. This continues to push miniaturization to an even greater level, therefore creating assemblies with smaller component and greater density.<br><br>Soldering materials, such as solder paste and flip-chip fluxes, will need to be chosen appropriately in order to form reliable solder joints and maximize production yields for complicated SiP applications. Fine feature solder paste printing for passive component sizes, down to 008004 (0.25 x 0.125mm) and smaller, or wafer level CSP (WLCSP) with small pad designs of less than 100µm in diameter, has become more challenging in SiP assembly. The appropriate choice of solder powder size, rheology of solder paste, and stencil design are crucial to achieve consistency in solder paste printing performance, which includes good printing transfer efficiency, minimal bridging down to 50µm gap between neighboring pads and at least 8 hours stencil life. Good wetting, graping resistance, and minimal voiding are some of the key attributes of solder paste to consider as well.<br><br>On the other hand, as technology drives toward finer pitch components, combined with reduced bondline thickness or standoff of flip-chip or other IC packages, makes cleaning flux residue more challenging. The shift towards using semiconductor-grade ultra-low residue no-clean flip-chip fluxes or solder pastes, which eliminates the cleaning process, is therefore the solution for overcoming these challenges. The flux residue left behind after the soldering process is minimal and compatible with the underfill or molding material used in the subsequent process.<br><br>This presentation will address the challenges and discuss basic guidelines in detail with testing results, for selecting appropriate solder pastes and flip-chip fluxes based on different SiP designs and requirements in the packaging industry. |

| Biography | |
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| | Sze Pei Lim is the Regional Product Manager for Semiconductor Material, and is based in Malaysia. She manages the semiconductor product lines for the Asia region and works closely with the local sales team and R&D to understand and develop solutions for industry needs and requirements. Some of her recent work includes close collaboration with customers in developing materials and process, for wafer/panel level ball attach application, fine feature printing targeted at the SiP application, as well as for one step OSP ball attach application.<br><br>Sze Pei joined Indium Corporation in 2007. She previously served as the Technical Manager for the Technical Support team in Southeast Asia.<br><br>Prior to joining Indium Corporation, Sze Pei was a research and development chemist. Her research included solder paste and flux formulation. She also worked as a technical manager for nine years for Inventec, where she provided technical support and managed testing in the lab.<br><br>Sze Pei has more than 25 years of experience mainly in the areas of semiconductor packaging assembly and surface mount technology. She earned her bachelor's degree from the National University of Singapore, majoring in industrial chemistry with a focus in polymers. Sze Pei is an SMTA-certified Process Engineer and has earned her Six Sigma Green Belt. |