Abstract & Biography: Electronics Assembly Technologies Forum by Surface Mount Technology Association (SMTA)

Moderator

Speaker	Mr. LOY Ter Chuen
Company	KYZEN, Malaysia
Designation	Sales & Technical Manager
Biography 	TC Loy is the Sales & Technical Manager at KYZEN. KYZEN is the leading provider of green engineered fluids and processes for precision cleaning applications in high-reliability manufacturing environment. Loy graduated with honors from Liverpool John Moore's University in Electronics Engineering and has 13 years of experience in the Electronics and Semiconductor Assembly Industry. He is based in Penang and supports Electronics and Semiconductor manufacturers in Northern Malaysia in developing and maintaining cleaning processes. He is also the current Treasurer of the SMTA Penang Chapter.

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Moderator

Speaker	Mr. Jonas SJOBERG
Company	Indium Corporation, Singapore
Designation	Asia Technical Manager
Biography 	Jonas Sjoberg is the Asia Technical manager at Indium Corporation with more than twenty years of experience in electronics assembly and packaging. During his carrier he have been initiating and driving Technology & Process development & improvement projects globally within Indium Corporation and various EMS, ODM & OEM. He have developed processes and guidelines for technologies such as 01005, ACF(Anisotropic Conductive Film), PoP (Package on Package), 0.30-0.40mm pitch CSP's (Chip Scale Packages), underfill and flip chip all for lead & halogen free assembly to meet worldwide environmental legislations.

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Professional Development Course

(08:30-12:00hrs)

Speaker	Dr. John LAU
Company	ASM Pacific Technology, Hong Kong
Designation	Senior Technical Advisor
Biography	With more than 37 years of R&D and manufacturing experience in semiconductor packaging, John has published more than 440 peer-reviewed papers, 30 issued and pending patents, and 18 textbooks on, e.g., Advanced MEMS Packaging (McGraw-Hill Book Company, 2010), Reliability of RoHS compliant 2D and 3D IC Interconnects (McGraw-Hill Book Company, 2011), TSV for 3D Integration, (McGraw-Hill Book Company, 2013), and 3D IC Integration and Packaging (McGraw-Hill Book Company, 2016). John is an elected ASME Fellow and has been an IEEE Fellow since 1994.
Title of Presentation	**Flip Chip, WLCSP, and FOWLP Assembly and Reliability**

Abstract

The major trend in the electronic industry today is to make products such as smartphones, tablets, wearables, internet of things, etc. more personal by making them smarter, lighter, smaller, thinner, shorter, and faster, while at the same time making them more friendly, functional, powerful, reliable, robust, innovative, creative, and less expensive. As the trend towards miniature and compact products continues, the introduction of cool products that are more user-friendly and contain a wider variety of functions will provide growth in the market. Some of the key technologies that are helping to make these cool product design goals possible are flip chip, WLCSP (wafer-level chip scale package), and FOWLP (fan-out wafer-level packaging). Their PCB (printed circuit board) assembly and solder joint reliability will be presented and discussed in this lecture. Since wafer bumping is the mother of flip chip and WLCSP technologies, it will be briefly mentioned first.

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Technical Program

(13:30-14:00hrs)

Speaker	Mr. Steve HURSEY
Company	Nordson Dage X-ray, UK
Designation	Business Development Manager
Biography	Steve Hursey is the Business Development Manager for Nordson Test & Inspection Division including DAGE X-ray, with responsibility in technically supporting Sales & Applications to Distribution Network and Customers direct. Steve has been involved in X-ray technology for over 30 years and is a renowned speaker internationally with published articles within Electronics journals. From full In-line AXI to High Resolution 3D CT X-ray, Steve has been working on providing solutions to many Manufacturing Companies in Semiconductor & Printed Circuit Assembly Globally. \Steve Hursey is qualified with a HND in Electrical/Electronic Engineering from Thames Valley University.
Title of Presentation	**Versatility in X-ray Inspection for the Electronics Manufacturing Industry**

Abstract

As technology moves in to a new level of ever shrinking dimensions, and ever-increasing complexity, the requirements for the X-ray inspection microscope needs consideration in its system configuration.

Whether used for Electronic Manufacturing of Printed Circuit Board Assembly, (PCBA) or for Semiconductor Manufacture, the fundamental components that make up the inspection system will vary in operation and design.

With the need for High Resolution X-ray to qualify the image integrity, at the smallest component geometry, the flexibility of the inspection technique needs to be considered to achieve the best utilization of the inspection system.

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Technical Program

(14:00-14:30hrs)

Speaker	Ms. Yvonne YEO Chii
Company	IBM Singapore Systems Supply Chain Engineering, Singapore
Designation	Advisory Engineer
Biography	Ms Yvonne Yeo is currently the Advisory Engineer from IBM Systems Supply Chain Engineering organization with 18 years' experience in semiconductor technology and supply chain operation. She joined IBM from 2008 and has various roles in supply chain engineering management for electronic components, supplier quality management, and technology qualification of logic and memory technologies. Her current role focuses on advanced memory technology qualification and data analytics initiatives for end to end memory quality management. She is also a lead auditor in the organization whereby her responsibilities cover supplier audits in Asia Pacific region. Yvonne graduated from the University of Canterbury, New Zealand with a Bachelor Degree (Honours) in Electrical and Electronics Engineering. Prior to IBM, she was a reliability engineer at XFAB Sarawak Sdn Bhd , responsible for wafer level reliability testing and process qualification. She has technical paper publications in various conferences such as IEEE, SMTA and ESD Symposium.
Title of Presentation	**A Holistic Approach for Technology and Quality Audits in the New Era of Computer Servers Design and Manufacturing**

Abstract

Supplier audits have played an essential role in supplier technology qualification and supplier quality assurance for many generations of hardware offerings, including computer servers, storage systems, and associated computer hardware products. Most recently, IBM's hardware offerings have focused on the enablement of cloud computing, big data and data analytics, mobile transactions, and cognitive computing. The complexity of system design and technology integration has increased tremendously for these product offerings. In addition, it's important to note that the electronics hardware supply chain has been undergoing substantial consolidation over this same period. Therefore, it is important to ensure the relevance of the approach and practice of supplier audits, so that supplier audits would continue to effectively mitigate quality risks for future generations of product offerings.

This paper introduces a holistic approach to enhance the effectiveness of technology qualification and quality assurance audits to address the challenges in both internal design complexity and external industry dynamics. The approach focuses on streamlining governing processes in audit execution and auditor training, as well as on IT and mobile applications development that further enables streamlining. To illustrate these points, this paper presents examples and case studies from electronic card assembly and test (ECAT) audits conducted across several contract manufacturing suppliers.

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Technical Program

(14:30-15:00hrs)

Speaker	Mr. Justin KOW
Company	Feinfocus Product Line, YXLON International, Singapore
Designation	Sales Manager
Biography	Sales manager for YXLON International GmbH, Feinfocus Product Line since 2014. I am based in Singapore and covering the business and marketing activities thru various distribution channels for South East Asia region. Previously I was working for a distribution company who handle different kind of semiconductor equipment both in front end (wafer) and back-end (packaging) processing for 15 years. One of the key fields I focus was in non-destructive testing technique such as x-ray, ultrasound for semiconductor packaging failure analysis.
Title of Presentation	**New LED Technology Challenges for X-Ray**

Abstract

Recent advances in LED technology have placed increased demands on the joint interfaces and materials used during production. Higher power, smaller size and increased reliability requirements intensify the need for higher quality more consistent production output. Flaws in the products can no longer be accepted as the performance requirements have increased dramatically, high power means higher temperatures and this needs very good thermal conductivity to move heat away from the key areas allowing the LED to last longer, as heat stresses the interfaces causing delamination or die fractures. Poor bond joints mean less transmission of power and this will reduce the life time of the components or their ability to perform at the required level. Many LEDs are potted or encapsulated and after this process the only non-destructive test option is x-ray, so as the requirement for LED inspection grows the need for high quality x-ray systems increases. This presentation will look at the common LED faults, most of which are only visible using x-ray technology and show good pass and fail images, also some of the recent technology advances in x-ray which make these images possible. Voiding is becoming more relevant too as there is a direct correlation between voids and thermal transfer and therefore reliability and product lifetime. We will look at technology which allows measurement of voids in individual interface areas of the assembly at the same time and see a video of an automated inspection routine measuring different areas on individual LEDs which are assembled onto a printed circuit board and how the voiding percentage in each area can be compared to pre-set acceptable limits. The concluding part of the presentation will include some 3D computer tomography images which could best be described as e micro-sections, these reconstructed images can be zoomed and cut though in any direction allowing the operator to look at any features within the structure. This technology produces great and very detailed images and with the latest powerful reconstruction and manipulation software allows the user to see details not previously seen before.

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Technical Program

(15:30-16:00hrs)

Speaker	Mr. Jeffrey LEN
Company	Indium Corporation, Malaysia
Designation	Senior Technical Support Engineer
Biography	Jeffrey Len is a Sr. technical support engineer for Indium Corporation and is based in Penang, Malaysia. He is responsible for providing comprehensive technical advice in the selection, use, and application of Indium Corporation's entire range of products to customers in Malaysia and Indonesia. Jeffrey's previous experience includes improving processes to increase output quality, and developing customer relationships to better service individual needs. Jeffrey holds a bachelor's degree in pure chemistry from Universti Sains Malaysia in Penang, Malaysia. Additionally, he is an SMTA-certified process engineer.
Title of Presentation	**Impact of Stencil Quality on Solder Paste Printing Performance**

Abstract

The growth of internet of thing (IOT) segment has induced much miniaturization development on the packaging and board level assembly. As the industry are moving to smaller and finer pitch such as 008004 , 0.3mm CSP and BGA, screen printing becomes one of the critical processes in the assembly to produce good quality surface mount assembly. It has been widely accepted that 50-70% of SMT defect come from printing application. There are a lot of variable that will impact the quality of printing such as machine set up, solder paste handling & storages, stencil quality, stencil aperture design, printing parameter and others. In this paper, we will evaluate the impact of stencil quality statistically through MiniTab software by comparison printing performance of different stencil supplier in 0.35mm pitch and 01005 pads.

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Technical Program

(16:00-16:30hrs)

Speaker	Mr. Guan Tatt YEOH
Company	ZESTRON Precision Cleaning Sdn Bhd, Malaysia
Designation	Senior Application Engineer
Biography	Guan Tatt Yeoh, is a Senior Application Engineer at ZESTRON South Asia. He has presented numerous technical papers and studies at trade shows and technical forums throughout South Asia. He is an active member of the SMTA. Mr. Yeoh received his diploma in Electrical & Electronics Engineering from Silicone Institute of Technology, Malaysia. He has been with ZESTRON SA since 2009 and he has worked continuously within the electronics assembly equipment industry since 1997, mainly in Semiconductor Industry, Machinery and Equipment Industry.
Title of Presentation	**PCB Surface Finishes & The Cleaning Process - A Compatibility Study**

Abstract

All PCBs that are manufactured require a surface finish to protect exposed copper on the surface which if left unprotected, can oxidize, rendering the board unusable. To address this issue, it is common to surface treat the PCB prior to assembly and reflow. The surface finish not only prevents oxidation of the underlying copper, but guarantees a solderable surface. A cost effective and widely used approach to PCB surface finish is HASL (Hot Air Solder Leveling). However, as circuit complexity and component density have increased, HASL has reached its limitations, necessitating the need for thinner coatings. Thus, coatings such as Immersion Tin (ImSn), Immersion Silver (ImAg), Organic Solderability Preservatives (OSP), and Electroless Nickel Immersion Gold (ENIG) are becoming more widely used.

As most PCBs designed for use in high reliability applications are cleaned in aqueous-based cleaning systems, the effect of the cleaning solution on the surface finish is of great concern. Depending on the cleaning process employed, stains could appear on the plating or in the worst case, the plating can be completely stripped from the PCB rendering the applied surface finish useless.

This study was designed to investigate the effect of reflow and various cleaning agent types on ImSn, ImAg and ENIG surface finishes. Unpopulated ZESTRONŽ test vehicles, with the appropriate surface finish, were used for all trials. Two alkaline cleaning agents, inhibited and uninhibited, and one pH neutral cleaning agent were used. Cleaning system process variables were established and held constant for all trials.

Surface finish assessment following reflow and cleaning was conducted using visual inspection, adhesion test, copper test (ImAg and ImSn), nickel test (ENIG), and the X-Ray Fluorescence (XRF) test. Additionally, baseline tests were conducted on boards without exposure to reflow or the cleaning process in order to assess the effect of the reflow process.

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Technical Program

(16:30-17:00hrs)

Speaker	Mr. Chwee Liong TEE
Company	Intel Products (M) Sdn Bhd, Malaysia
Designation	Senior Test Engineer
Biography	Structural test architect responsible in path finding and validating new board test technology. Ensure smooth deployment of test strategy across factories. Papers presented at IEEE International Test Conference: 1. Augmenting Board Test Coverage with New Intel Powered Opens Boundary Scan Instruction (2009) IEEE International Test Conference 2. Challenges of Implementing Bead Probe Technology (BPT) in High Volume Manufacturing (HVM) 3. Impact of Quad Flat No Lead package (QFN) on automated X-ray inspection (AXI). 2007
Title of Presentation	**Improving Automatic X-Ray Inspection Process with Artificial Intelligence**

Abstract

Automatic X-ray Inspection (AXI) is widely used in the PCB assembly process to detect manufacturing defects as well as provide feedback for process improvement. With the proliferation of BGA and PoP packages, the importance of AXI is gaining more prominent. However, maintaining a robust AXI process is a challenge because it relies on human operator to make the final judgment to either Pass or Fail a board. It is a norm for human operator to review few hundreds of false calls images on each board. Base on observation, operator only spend about 1s to review each image so as to keep up with the output which could lead to escapes. Escapes could also be due to human fatigue. Not only that, human judgment varies depending on the knowledge and experience.

Lately Artificial Intelligence (AI) is in vogue. Various solutions have been thought of revolving around AI. Although AI is an emerging technology, there has been tremendous breakthrough in hardware, software model coupled with huge amount of dataset generated by factory, we think that AI can be an effective tool in improving the factory PCB assembly process.

We initiated this project to demonstrate that the number of AXI false calls to be reviewed by operator can be reduced with the introduction of AI. Our AI model is able to hit above 90% accuracy. It is also able to detect some of the escapes judged by the operator. We will share what are the strategies and preparation needed to implement AI. We will discuss about the quality of dataset and its impact to the accuracy of the AI model. Also shared are benchmark results of the various AI models.

We would also like to propose to the industry on how we can accelerate the adoption of AI to improve the factory PCB assembly process.